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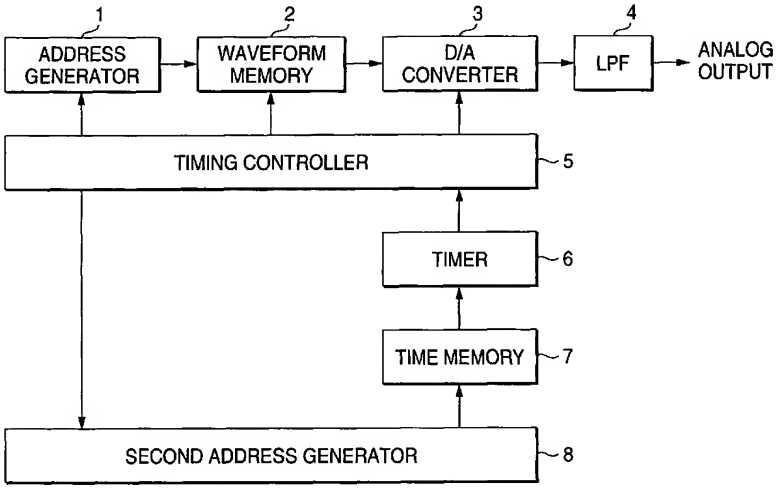
(54) WAVEFORM GENERATION METHOD, WAVEFORM GENERATION PROGRAM, WAVEFORM GENERATION CIRCUIT, AND RADAR DEVICE

(57) A conventional waveform generation circuit was required to increase a number of bits or a sampling rate for a D/A converter to enhance a precision of waveform shaping, and had a problem that a cost was increased. Therefore, as a method for enhancing the precision of waveform shaping, a quantization error of an output waveform is made smaller by controlling an output time interval of an output value from a D/A converter so as to make a difference in an output voltage between target waveform and output waveform smaller. As a result, even if the D/A converter has a small number of bits, the waveform can be generated at high precision. Also, this waveform generation method may be applied to modulation control of a radar apparatus, as a result, constituting a small and inexpensive modulation circuit for an oscillator.

FIG. 4



EP 1 533 906 A1

Description

TECHNICAL FIELD

[0001] The present invention relates to a waveform generation method, a waveform generation program, and a waveform generation circuit for generating a waveform in programmable manner, and a radar apparatus having the waveform generation circuit as a modulation circuit.

BACKGROUND ART

[0002] A conventional circuit for reproducing an analog waveform by converting a digital signal into an analog signal, including a D/A (Digital to Analog) converter for decoding and step-pulsing, and a post-filter (identical to a low pass filter), has been well known. This circuit involved a quantization error from a desired target waveform in a range from -1/2LSB to +1/2LSB (e.g., refer to Iwao Sagara, "Introduction to AD/DA Conversion Circuit, P.68 to P.75, P.80 and P.81).

[0003] Fig. 11 is a block diagram showing one example of the conventional waveform generation circuit. In Fig. 11, 1 denotes an address generator for generating the address value of a memory, and 2 denotes a waveform memory for storing waveform data. 3 denotes a D/A (Digital to Analog) converter for converting a digital value into an analog value in accordance with an output value of the waveform memory 2, and 4 denotes a low pass filter for removing high frequency components of output of the D/A converter 3 to make the waveform smoother. 5 denotes a timing controller for supplying necessary control signals such as a clock signal and an enable signal to the address generator 1 and the D/A converter 3. This waveform generation circuit may be employed as a speech synthesis unit by adding an amplifier for amplifying power and a speaker.

[0004] In Fig. 11, the waveform memory 2 preliminarily stores waveform data desired to generate waveform, the waveform data being arranged in time series. The timing controller 5 generates a control signal such as a trigger signal to output a memory address value to the address generator 1 at regular time intervals. The timing controller 5 generates a control signal such as a chip select signal required for memory output to the waveform memory 2, and outputs a trigger signal or a select signal required for D/A conversion to the D/A converter 3.

[0005] The address generator 1 outputs the address value in the order from the initial address of waveform data stored in the waveform memory 2 in synchronism with a trigger signal received from the timing controller 5 at regular time intervals. The waveform memory 2 outputs waveform data according to the address value output from the address generator 1. The D/A converter 3 outputs a voltage proportional to a value output from the waveform memory 2, if the value is set. The low pass filter (LPF) 4 removes a sampling noise produced in accordance with an output period of the D/A converter 3.

[0006] Fig. 12 shows the basic concept of a waveform generation method for use with the conventional waveform generation circuit. In Fig. 12, 101 is a target waveform to be generated, and 104 denotes a D/A output waveform. The conventional waveform generation circuit determined the output by performing a so-called quantization involving selecting a value of the D/A converter closest to a waveform value of analog quantity at a regular interval sampling time Ts, if the target waveform 101 was given. The D/A output waveform 104 represents the output voltage values in time series, which are supplied from the D/A converter 3 at regular intervals.

[0007] Fig. 13 is an enlarged view of Fig. 12. In Fig. 13, an output point 102 of the D/A converter 3 is selected at a value close to the target waveform, but a quantization error δ as large as 1/2 LSB at maximum occurs at the regular interval sampling time Ts, as compared with a transit point 103 of the target waveform at the same point of time. That is, the quantization error δ falls in a range from -1/2 LSB to +1/2 LSB.

[0008] Fig. 14 is a block diagram showing one example of the configuration of an FM-CW radar apparatus. Herein, 801 denotes a modulation circuit, 802 denotes an oscillator, 803 denotes a directional coupler, 804 denotes a transmission antenna, 805 denotes a reception antenna, 806 denotes a mixer, 807 denotes an amplifier, 808 denotes an A/D (Analog to Digital) converter, 809 denotes frequency analysis means, 810 denotes target detecting means, and 811 denotes distance/speed calculating means (e.g., refer to S. A. Hovanessian, "Radar System Design & Analysis", Artech House, INC., p.78 to p.81).

[0009] In Fig. 14, first of all, the modulation circuit 801 generates a frequency modulation (hereinafter referred to as FM (Frequency Modulation)) signal, which is sent to the oscillator 802. The oscillator 802 generates a high frequency signal modulated with the FM signal and the high frequency signal being distributed by the directional coupler 803 is sent to the transmission antenna 804 and the mixer 806. The transmission antenna 804 radiates a transmitting wave of the high frequency signal toward a target object in front of the radar apparatus. Herein, when the target object exists, a receiving wave (reflected wave) with a time lag is received by the reception antenna 805, and sent to the mixer 806. The mixer 806 generates a signal of frequency difference (hereinafter referred to as a beat signal) between this reflected wave and the transmitting wave distributed by the directional coupler 803. This beat signal is sent to the amplifier 807. The amplifier 807 amplifies the beat signal, and then sent to the A/D converter 808.

[0010] The A/D converter 808 converts the beat signal from analog to digital signal form, the beat signal in digital form is then sent to the frequency analysis means 809. The frequency analysis means 809 inputs the dig-

itized beat signals and provides a frequency distribution (frequency spectrum) through the processing of FFT (Fast Frequency Transform) etc. The target detecting means 810 compares the frequency distribution with a threshold, and detects the target value as the largest one of the values beyond the threshold. The distance/speed calculating means 811 calculates the relative distance and relative speed of the target object based on a frequency picked up by the target detecting means 810.

[0011] Fig. 15 and Figs. 16(a) and 16 (b) are views for explaining how to calculate the relative distance and relative speed of the target object. Fig. 15 shows variations in the frequency, and Figs. 16(a) and 16(b) show a frequency spectrum of the beat signal simply. In Fig. 15, 812 denotes a transmitting frequency of the FM-CW radar apparatus, and 813 denotes a receiving frequency.

[0012] First of all, the transmitting frequency 812 is linearly increased in an UP chirp interval Tmu, and linearly decreased in a DOWN chirp interval Tmd to transmit electric wave. Herein, it is supposed that a measuring object exists at the relative speed v and the relative distance R to the FM-CW radar apparatus. At this time, if the transmitting frequency is changed by Δf at the light speed C [m/s] and the transmitting wavelength λ[m] in the time intervals Tmu and Tmd, the Doppler frequency fd is represented by a function (1). Herein, the distance frequency fr caused by a time difference between the transmitting frequency and the receiving frequency, which is proportional to the distance, is represented by a function (2). Also, the beat frequency fb1 in the Up chirp interval Tmu and the beat frequency fb2 in the DOWN chirp interval Tmd are represented by functions (3) and (4), respectively.

$$fd = 2 \cdot V/\lambda \quad (1)$$

$$fr = (2R \cdot \Delta f)/(C \cdot Tm) \quad (2)$$

$$fb1 = |fd - fr| \quad (3)$$

$$fb2 = |fd + fr| \quad (4)$$

[0013] Also, when the distance frequency fr is greater than the Doppler frequency fd, a function (5) holds.

$$2fr = fb1 + fb2 \quad (5)$$

[0014] By the way, substituting the function (2) for the function (5), a function (6) for calculating the relative distance from the FM-CW radar apparatus to the target object is derived.

$$R = (C \cdot Tm) \cdot (fb1 + fb2)/(4 \cdot \Delta f) \quad (6)$$

[0015] From the function (6), the distance to the target object is calculated from the beat frequency fb1 in the UP chirp interval Tmu and the beat frequency fb2 in the DOWN chirp interval Tmd. Also, if the distance frequency fr is calculated, the relative speed V is obtained from the functions (1), (3) and (4).

[0016] The conventional radar apparatus for measuring the distance with the FM modulation supplies a voltage of staircase shape to a voltage controlled oscillator to improve the distance measurement precision. At this time, the frequency measuring means measures an output frequency from the voltage controlled oscillator. The frequency measuring means measures the output frequency from the voltage controlled oscillator, corresponding to each voltage of staircase shape, and calculates an applied voltage for making the -sweep speed invariable from this measured frequency. Control means operated the distance measurement by supplying this applied voltage to the voltage controlled oscillator at a predetermined interval. (e.g., refer to JP-A-2002-156447).

DISCLOSURE OF INVENTION

[0017] The conventional waveform generation circuit produced a quantization error of 1/2LSB at maximum from the target waveform if the output control for the D/A converter is made at an equal time interval. Also, when a micro signal is dealt with, a periodical ripple noise occurred due to the quantization error of the D/A converter.

[0018] Figs. 17(a) and 17(b) show how the ripple noise occurs due to the quantization error. Fig. 17 (a) shows the relationship between the target waveform and the D/A output waveform, and Fig. 17 (b) shows the relationship between the D/A output waveform and the output waveform of the low pass filter. For the simplified explanation, the target waveform is linear. 901 denotes a target waveform, 902 denotes a D/A output waveform output from the D/A converter 3 by quantizing the target waveform 901, and 903 denotes the output of the low pass filter 4 disposed at the latter stage of the D/A converter 3 and provided to remove the sampling noise.

[0019] As seen from Fig. 17(a), when the minimum step width of the quantization output is rough relative to the target waveform 901, the error between the output voltage of the D/A converter 3 and the target waveform is periodically greater. As a result, the output waveform is undulated as indicated by the output 903 of the low pass filter 4 in Fig. 17 (b), so that a ripple noise of the low frequency that is the sampling frequency divided by an integer (1/4, 1/5, etc.) appears superposed on the ideal target waveform.

[0020] Conventionally, it was required to increase the number of bits or the sampling frequency in the D/A converter to reduce this ripple noise, so that the cost was

increased.

[0021] Also, the FM-CW radar apparatus for measuring the distance by applying the frequency modulation was required to make the high precision modulation control, but if the modulation signal has the superposed ripple noise, the beat signal as a difference between the transmitting wave and the receiving wave was distorted, causing the frequency spectrum to split or the other peak to arise at a position off the center of the frequency spectrum.

[0022] Figs. 18(a), 18(b) and 18(c) are graphs showing the frequency spectrum of the beat signal for the FM-CW radar apparatus. 904 denotes a frequency spectrum of the beat signal in the UP chirp or the DOWN chirp. When the transmitting frequency is linearly changed, the beat signal is stable and has one frequency, and the peak value appears sharply as indicated by the frequency spectrum 904 in Fig. 18(a), and then the peripheral portion is at the side lobe level following a window function.

[0023] However, if the transmitting frequency is not correctly linear but has the superposed ripple noise, another peak appears at a position off the peak frequency by an amount of frequency according to the period of ripple noise.

[0024] Fig. 18 (b) shows an instance where the frequency of ripple noise is near the resolution of spectrum, and the maximal point arises halfway on the spectrum of the beat signal. Fig. 18(c) shows an instance where the ripple frequency is higher and sufficiently away from the spectrum of the beat signal. In Figs. 18 (b) and 18 (c), there is an obstacle to calculate the distance to the target object.

[0025] Conventionally, the D/A converter for use in the modulation circuit for the FM-CW radar apparatus was required to increase the number of bits or the sampling number to make the high precision control. Therefore, the cost was increased.

[0026] This invention has been achieved to solve the above-mentioned problems, and it is an object of the invention to provide a waveform generating method of high precision in which the ripple noise is suppressed.

[0027] Also, it is another object of the invention to provide a waveform generation circuit of small size and low cost and a radar apparatus having the waveform generation circuit in a modulation circuit.

[0028] According to one aspect of the invention, there is provided a waveform generation method including, for a desired target waveform output from a D/A converter, determining preliminarily an output value and an output timing of the D/A converter so that a voltage variation amount of the target waveform may be almost constant, and sequentially generating the output value from the D/A converter, based on the determined output value and output timing of the D/A converter.

[0029] According to another aspect of the invention, there is provided a waveform generation circuit including a time memory for storing an output time interval of the waveform output values preset discretely based on a desired target waveform, a timing controller for setting up the timing at which the D/A conversion of the waveform output value is performed, based on the output time interval stored in the time memory, and a D/A converter for performing the D/A conversion of the waveform output value according to the timing set up in the timing controller.

BRIEF DESCRIPTION OF DRAWINGS

[0030]

Figs. 1(a), 1(b), 1(c), 1(d) and 1(e) are graphs for explaining a waveform generation method according to an embodiment 1 of this invention.

Fig. 2 is a graph for explaining reduction of an error between target waveform and output waveform from the D/A converter according to the embodiment 1 of the invention.

Figs. 3(a), 3(b) and 3(c) are graphs for explaining the relationship between the gradient of target waveform and the output time interval according to the embodiment 1 of the invention.

Fig. 4.is a block diagram showing the configuration of a waveform generation circuit according to an embodiment 2 of the invention.

Fig. 5 is a block diagram showing the configuration of a waveform generation circuit according to an embodiment 3 of the invention.

Fig. 6 is a flowchart showing a data creation processing procedure according to the embodiment 3 of the invention.

Figs. 7 (a) and 7 (b) are tables showing the memory contents according to the embodiment 3 of the invention.

Fig. 8 is a diagram for explaining a way of setting up the output time interval from the target waveform according to the embodiment 3 of the invention.

Fig. 9 is a flowchart showing a waveform output processing procedure according to the embodiment 3 of the invention.

Figs. 10(a) and 10(b) are graphs showing the modulated waveform of a radar apparatus according to an embodiment 4 of the invention.

Fig. 11 is a block diagram showing the configuration of the conventional waveform generation circuit.

Fig. 12 is a graph showing a waveform generation method for the conventional waveform generation circuit.

Fig. 13 is a diagram for explaining an error between the target waveform and the D/A converter output in the conventional waveform generation circuit.

Fig. 14 is a block diagram showing an FM-CW radar apparatus.

Fig. 15 is a graph showing a transmitting waveform and a receiving waveform for the FM-CW radar apparatus.

Figs. 16(a) and 16(b) are graphs showing the frequency spectrum of a beat signal.

Figs. 17 (a) and 17 (b) are graphs for explaining a problem associated with the conventional waveform generation circuit.

Figs. 18(a), 18(b) and 18(c) are graphs for explaining a problem associated with the conventional FM-CW radar apparatus.

BEST MODE FOR CARRYING OUT THE INVENTION

[0031] The present invention will be described below in detail with reference to the accompanying drawings.

Embodiment 1

[0032] Figs. 1(a), 1(b), 1(c), 1(d) and 1(e) are a set of graphs showing a waveform generation method according to an embodiment 1 of this invention. In Figs. 1(a), 1(b), 1(c), 1(d) and 1(e), 101 denotes a target waveform, 102 denotes a threshold voltage, 103 denotes an intersection point of the threshold voltage 102 and the target waveform 101, and 104 denotes a D/A output waveform.

[0033] Referring to Figs. 1(a), 1(b), 1(c), 1(d) and 1 (e), the operation of the embodiment 1 will be now described.

[0034] The target waveform 101 in Fig. 1 (a) is an ideal waveform without error that is essentially desired to output, or a sufficiently finely approximated waveform. Suppose that the target waveform 101 is preliminarily given by another measurement means or calculation, not shown.

[0035] If the quantization interval (voltage direction) and the output time interval (time direction) are rough, the D/A converter cannot directly output the same waveform as the target waveform 101. Therefore, it is required to determine a combination of output values from the D/A converter to acquire an output waveform close to the target waveform 101. In the embodiment 1, an error between the output waveform and the target waveform 101 is reduced by making the output time interval of the D/A converter 3 variable.

[0036] A method for determining the output value of the D/A converter 3 and the output time interval will be described below.

[0037] Fig. 1 (b) shows how to divide the target waveform 101 based on plural threshold values 102 represented with the D/A converter 3 in use. The threshold voltages 102 are set up from the minimum value to the maximum value of the D/A converter 3 at a voltage step of the minimum resolution for the D/A converter 3. This minimum resolution is decided by the number of bits for the D/A converter 3. First of all, the output values of the D/A converter 3 are obtained from a plurality of intersection points 103 at which the threshold voltage 102 and the target waveform 101 are coincident, as shown in Fig. 1 (c). The output values of the D/A converter 3 are v1, v2, .. vn in the order in which the intersection point 103 take place earlier over time.

[0038] Then, the output time interval is decided. The output time is acquired by reading the value in the time axis direction from the intersection point 103, and deciding the time t1, t2, ..tn corresponding to v1, v2, ..vn, as shown in Fig. 1(d). The output time interval is defined such that the time difference is T1 from reference time to t1, T2 from t1 to t2, .. (omitted) and Tn from tn-1 to tn. Suppose that T1 to Tn are rounded off to the integral multiple of a clock period for a microcomputer.

[0039] Fig. 1 (e) is a graph for explaining how the D/A converter 3 makes the waveform output by the waveform generation method according to the embodiment 1. That is, the D/A output waveform 104 of the D/A converter 3 is changed in succession based on the decided output values v1, v2, .. vn and output time interval T1, T2, .. Tn. The value of the D/A converter 3 is kept constant until the D/A output waveform is changed. The D/A output waveform 104 of the D/A converter 3 is like a staircase, containing an error from the target waveform 101. However, a low pass filter for delaying the response purposely is disposed on the output side of the D/A converter 3, as a result, blunting a staircase edge in the output of the D/A converter 3 (interpolating between the staircase like output values), so that the final output from the low pass filter is closer to the target waveform 101.

[0040] In the first embodiment 1, the output time interval is set longer when the waveform is changed slowly, or shorter when the waveform is changed sharply, so that an error from the target waveform can be reduced to the least.

[0041] Fig. 2 is an enlarged view of Figs. 1(a), 1 (b), 1(c) 1 (d) and 1(e) showing how an error between the target waveform and the output of the D/A converter is reduced. In Fig. 2, 201 denotes an output point (at which a specific output voltage is obtained at a specific output time) of the D/A converter 3 in the conventional waveform generation circuit, 202 denotes a transit point of the target waveform at the same point of time as the output point 201, and 203 denotes an output point of the D/A converter 3 decided by the method of the embodiment 1. A quantization error δ between the output point 201 of the D/A converter 3 in the conventional waveform generation circuit and the transit point 202 of the target waveform is greater. However, in this embodiment 1, the position of output point is finely adjusted in the time direction at an integral multiple of the clock unit (clock interval) K of the microcomputer. At this time, the output time interval Tn is adjusted to the optimal interval to minimize a difference between the output point 203 of the D/A converter 3 and the output voltage at the transit point of the target waveform. As a result, a quantization error between the output point 203 of the D/A converter 3 and the output voltage at the transit point of the target waveform is reduced. In Fig. 2, the output point 203 of the D/A converter 3 roughly overlaps the transit point of the target waveform, so that the quantization error is extremely smaller.

[0042] Figs. 3 (a), 3 (b) and 3 (c) shows the instances of the linear target waveform in the embodiment 1. The slope of target waveform is gentlest in Fig. 3(a), and gradually greater in Fig. 3(b) and Fig. 3(c). With the method of the embodiment 1, even if the slope is changed from Fig. 3(a) to Fig. 3(c), the output time is appropriately adjusted at an integral multiple of the clock unit to regulate the output time interval, as a result, roughly eliminating the error between the target waveform and the output waveform of the D/A converter. Especially when the target waveform is linear, the greatest effect is obtained.

[0043] According to this embodiment, the quantization error of the D/A converter is smaller by changing the output time interval between the output points of the D/A converter than where the output interval is equal over time, so that the ripple noise of low frequency likely to occur with the micro signal is suppressed.

Embodiment 2

[0044] Fig. 4 is a block diagram showing the configuration of a waveform generation circuit according to an embodiment 2 of this invention. In Fig. 4, 1 denotes an address generator for generating the address value of a waveform memory, 2 denotes a waveform memory for storing waveform data, 3 denotes a D/A converter for converting a digital value into an analog value in accordance with an output value of the waveform memory 2, 4 denotes a low pass filter (LPF) for removing high frequency components of output of the D/A converter 3 to make the waveform smooth, 5 denotes a timing controller for supplying necessary control signals such as a clock signal and an enable signal to the address generator 1 and the D/A converter 3, 6 denotes a timer for triggering the timing controller 5, 7 denotes a time memory for storing the time interval data, and 8 denotes a second address generator for generating the address value of the time memory 7.

[0045] Referring to Fig. 4, the operation of the embodiment 2 will be described below.

[0046] In Fig. 4, the output voltage values v1 to vn set discretely as shown in the embodiment 1 are preliminarily stored in time series in the waveform memory 2. Also, the time memory 7 preliminarily stores the timer values corresponding to the output time intervals T1 to Tn as shown in the embodiment 1, for example, the count number of a reference clock. The timing controller 5 generates a control signal such as a trigger signal to output a memory address value to the address generator 1 and the second address generator 8 and outputs a trigger signal or select signal required for the D/A conversion to the D/A converter 3.

[0047] First of all, the timing controller 5 applies a trigger signal to the second address generator 8. Then, the second address generator 8 outputs the address value in the order from the initial address of the timer value stored in the time memory 7. From the time memory 7, the timer value is read according to the address value received from the second address generator 8, and set to the timer 6. The timer 6 supplies the trigger signal to the timing controller 5 at an interval according to the output time intervals T1 to Tn indicated by the set timer value. The timing controller 5 sends the trigger signal to the address generator 1, the waveform memory 2 and the D/A converter 3 in synchronism with the trigger signal received from the timer 6.

[0048] The address generator 1 outputs the address value in the order from the initial address of waveform data stored in the waveform memory 2 in synchronism with the trigger signal. The waveform memory 2 outputs waveform data in synchronism with the trigger signal, and sets it to the D/A converter 3. The D/A converter 3 outputs a voltage in proportion to the set value from the waveform memory 2 in synchronism with the trigger signal. The low pass filter 4 removes a sampling noise produced in accordance with an output period of the D/A converter 3. The waveform generation method as shown in the embodiment 1 is implemented by sending the trigger signal from the timing controller 5 to the second address generator 8 again, and repeating the series of operations.

[0049] With this embodiment, the output time interval is arbitrarily set in a clock unit, an error between the target waveform and the output waveform is suppressed below the quantization error of 1/2LSB produced with the conventional method for using the D/A converter, whereby it is unnecessary to take a great number of bits in the D/A converter. That is, the output waveform is generated at high precision, employing the inexpensive D/A converter with a smaller number of bits.

Embodiment 3

[0050] Fig. 5 is a block diagram showing the configuration of a waveform generation circuit according to an embodiment 3 of the invention. In Fig. 5, 3 and 4 are the same as in the embodiment 2. 9 denotes a microcomputer having an I/O for interface with the D/A converter 3, and a timer circuit for correctly setting up an interrupt generation time according to the timer value. In an internal memory of the microcomputer 9, the output voltage value of the D/A converter 3 and the timer value corresponding to the output time interval are stored.

[0051] Herein, a group of waveform generation features comprises the address generator 1, the waveform memory 2, the timing controller 5, the timer 6, the time memory 7, and the second address generator 8 in the embodiment 2 are internally stored as a software processing in the microcomputer 9, as a result, allowing the same operation as the embodiment 2 to be performed.

[0052] The software processing is divided into two parts, including a data creation processing for storing data in the time memory 7 and the waveform memory 2, and a waveform output processing. Fig. 6 shows the

data creation processing.

[0053] Also, Fig. 7(a) shows the contents of the time memory 7 and Fig. 7 (b) shows the contents of the waveform memory 2. Fig. 8 shows an explanatory view for obtaining the output time interval from the target waveform. Fig. 9 shows the waveform output processing.

[0054] Referring to Fig. 6, the data creation processing will be firstly described.

[0055] At step S101, the target waveform is approximated by a plurality of n-th order functions (n: integer) by dividing the waveform at smaller time intervals to make the approximation precision sufficiently high, because it is generally difficult to represent the target waveform with one function. 401 in Fig. 8 is an approximate target waveform approximated by a plurality of linear functions, for example.

$$v=f1(t)=a1\cdot t+b1 \text{ for } t001\leq t<t002$$

$$v=f2(t)=a2\cdot t+b2 \text{ for } t002\leq t<t003$$

$$v=f3(t)=a3\cdot t+b3 \text{ for } t003\leq t<t004$$

...

[0056] At step S102, an inverse function of the function generated at step S101 is calculated to acquire the time t for the voltage value that the D/A converter 3 can take.

$$t=(v-b1)/a1 \text{ for } v001\leq v<v002$$

$$t=(v-b2)/a2 \text{ for } v002\leq v<v003$$

$$t=(v-b3)/a3 \text{ for } v003\leq v<v004$$

...

v001, v002, .. are values obtained by substituting t001, t002, .. for the plurality of linear functions.

[0057] At step S103, the times t1 to tN for the set voltages v1 to vN of the D/A converter 3 are obtained. The range of the set voltages v1 to vN depends on the range of the target waveform, and the interval of voltage depends on the minimum quantized voltage ΔV of the D/A converter 3. For example, the set voltage is represented by the following function for n=1 to N.

$vn = v0+\Delta V\cdot n$ (v0 is the initial value of output voltage of target waveform).

[0058] Substituting this function for the inverse function calculated at step S102, the times t1 to tN are obtained. For which inverse function it is substituted depends on an area determination of v1, v2, ..

[0059] At step S104, the times t1 to tN are converted into time differences T1 to TN for conversion into the output interval of the D/A converter 3.

$$T1 = t1$$

$$T2 = t2-t1$$

$$T3 = t3-t2$$

...

[0060] Then, at step S105, the time differences T1 to TN are stored in the time memory 7. At step S106, the set voltages v1 to vN are stored. Zero is set at the top address of the time memory as the initial value, and the initial value v0 of output voltage of target waveform is stored at the top address of the waveform memory 2.

[0061] Referring to Fig. 9, the waveform output processing that is another software processing will be described.

[0062] First of all, at step S201, the initial value of zero is substituted for the loop variable n.

[0063] Then, at step S202, the n-th time data Tn is read from the time memory 7 and set to the timer internally built for the microcomputer 9.

[0064] Then, at step S203, the timer is initiated.

[0065] Then, at step S204, if a notification of the time elapsed is received from the timer, the n-th waveform data is read from the waveform memory 2, and set to the D/A converter 3. The timer at steps S202 and S203 may be implemented by the software processing for a dummy loop.

[0066] Then, at step S205, a determination is made whether or not the waveform output processing is completed. When it is not completed, the procedure goes to step S206, where the loop variable n is counted up.

[0067] The data creation processing may not be performed on the same microcomputer 9, but data may be preliminarily created on an external computer and written into the time memory 7 and the waveform memory 2 of the microcomputer 9. Also, when the waveform data is increased at a certain interval, a counter may be employed instead.

[0068] Though in this embodiment, the microcomputer is employed to make the software processing for the group of waveform generation features, other computers having the typical computer functions of logical operation and arithmetical operation, such as a personal computer, an office computer, a mini computer and a general-purpose computer, may be also employed.

[0069] With this embodiment, the waveform is generated at high precision employing the inexpensive D/A converter with a small number of bits, and the specifi-

cation changes for the software processing are easily made.

Embodiment 4

[0070] Figs. 10(a) and 10(b) are graphs showing the modulation waveform according to an embodiment 4 of this invention. In Fig. 10 (a), 501 denotes an UP chirp waveform of modulation waveform output from a modulation circuit 801 in the FM-CW radar apparatus, and 502 denotes a DOWN chirp waveform. In Fig. 10 (b), 503 denotes an output waveform of the D/A converter 3. This modulation waveform is generated by the waveform generation circuit as described in the embodiment 2 or 3. Also, this waveform generation circuit constitutes the modulation circuit 801 of the FM-CW radar apparatus, as shown in Fig. 14. The other constitution or basic operation of the FM-CW radar apparatus has been already described in connection with Figs. 14 to 16(a) and 16(b), and is omitted here.

[0071] For an oscillator of the FM-CW radar apparatus, it is required to apply a control voltage in accordance with the characteristics for each oscillator, because there is typically a non-linear relationship between control voltage (modulation waveform) and oscillation frequency, and also due to individual differences and temperature characteristics. The UP chirp waveform 501 and the DOWN chirp waveform 502 of Figs. 10(a) and 10(b) involve a control voltage waveform output from the modulation circuit 801 and applied to the oscillator. This control voltage waveform is generated to change the frequency linearly. For these waveforms, the output timings t1 to tn ($n \leq N$) at which the quantization error is smaller are obtained, and replaced with the output time intervals T1 to Tn of the D/A converter 3. Though the output time intervals T1 to Tn are unequal, the method for calculating these intervals has been described in the embodiments 1 to 3.

[0072] Also, an output voltage is output from the D/A converter 3 at the output time intervals T1 to Tn, whereby the oscillator is linearly oscillated and the frequency spectrum of target object is stabilized even if the control voltage is a micro signal. The waveform output operation of this D/A converter 3 (i.e., waveform generation circuit constituting the modulation circuit 801) is the same as that described in the embodiments 1 to 3.

[0073] In this embodiment, the waveform generation circuit as described in the embodiment 2 or 3 is applied as the modulation circuit for modulating the oscillation frequency for the oscillator constituting the FM-CW radar apparatus. As a result, the FM-CW radar apparatus including the small and inexpensive modulation circuit for the oscillator is constituted.

INDUSTRIAL APPLICABILITY

[0074] As described above, the waveform generation method, the waveform generation program and the waveform generation circuit according to the invention allow reduction of an error between the target waveform and the output waveform, in contrast to the case of outputting the signal at an equal time interval from the D/A converter to obtain a desired target waveform. Therefore, the FM-CW Radar apparatus including the small and inexpensive modulation circuit for the oscillator is constituted.

Claims

1. A waveform generation method comprising steps of:

   for a desired target waveform output from a D/A converter,
   determining preliminarily an output value and an output timing of the D/A converter so that a voltage variation amount of the target waveform may be almost constant; and sequentially generating the output value from the D/A converter, based on the determined output value and output timing of the D/A converter.

2. The waveform generation method according to claim 1, further comprising a step of:

   interpolating between the output values of the D/A converter while a low pass filter is provided on an output side of the D/A converter.

3. A program for generating a waveform employing data created in accordance with a procedure of steps (a) to (f) and stored in a time memory and a waveform memory, wherein

   the waveform is output in accordance with a waveform output processing procedure of steps (g) to (k);

   (a) a step of approximating a target waveform v with a plurality of functions f1(t), f2(t), f3(t), ..;
   (b) a step of calculating inverse functions of the plurality of functions f1(t), f2(t), f3(t), ..;
   (c) a step of acquiring times t1, t2, t3, ..tN corresponding to output set-up voltage values V1, V2, V3, .., Vn of a D/A converter;
   (d) a step of replacing the times t1, t2, t3, ..tN with time differences T1, T2, T3, ..TN between a current time and a previous time;
   (e) a step of storing the time differences T1, T2, T3, ..TN in the time memory, wherein an initial value T0 of the time difference is zero and stored at an address value 0000;
   (f) a step of storing the output set-up voltage values V1, V2, V3, .. in the waveform memory, wherein an initial value V0 of the waveform memory is stored at an address value 0000;

(g) a step of substituting an initial value of zero for a loop variable n;
(h) a step of reading a n-th time data Tn from the time memory and setting the time data Tn in a predetermined timer;
(i) a step of initiating and counting the timer;
(j) a step of accepting a count end notification from the timer, reading a n-th waveform data from the waveform memory, and setting the output set-up voltage value Vn in the D/A converter; and
(k) a step of determining a completion status of a waveform output process by confirming the loop variable n, and repeating a series of processing from step (h) to step (j) by counting up the loop variable n until completion.

4. A waveform generation circuit comprising:

a time memory for storing an output time interval of waveform output values preset discretely based on a desired target waveform;
a timing controller for setting up a timing at which a D/A conversion of the waveform output values is performed, based on the output time interval stored in the time memory; and
a D/A converter for performing the D/A conversion of the waveform output values according to the timing set up in the timing controller.

5. The waveform generation circuit according to claim 4, further comprising:

a low pass filter for interpolating between output values of the D/A converter.

6. A radar apparatus comprising:

the waveform generation circuit according to claim 4 or 5 as a modulation circuit for modulating the oscillation frequency of an oscillator.

FIG. 1(a)

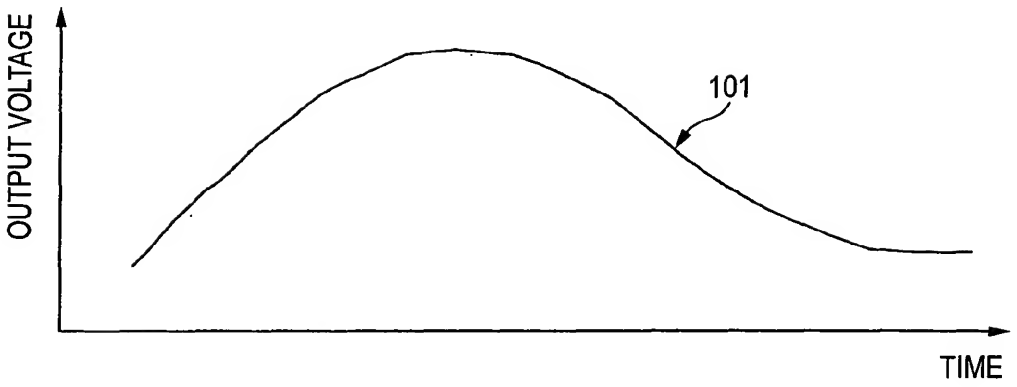


FIG. 1(b)

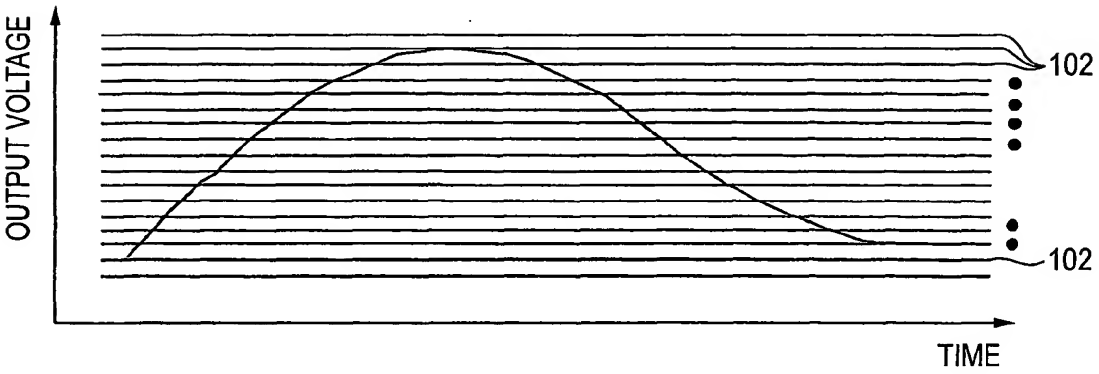


FIG. 1C

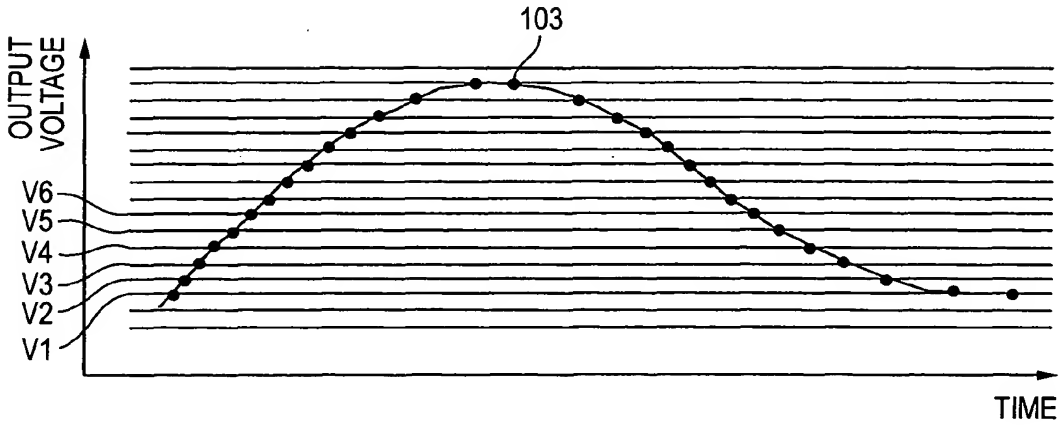

103
OUTPUT VOLTAGE
V6
V5
V4
V3
V2
V1
TIME

FIG. 1D

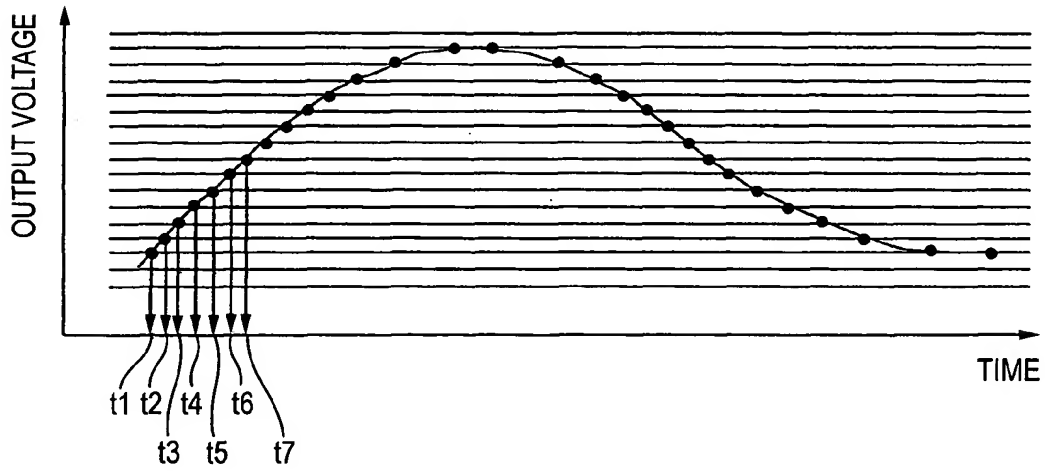

OUTPUT VOLTAGE
TIME
t1
t2
t3
t4
t5
t6
t7

FIG. 1(e)

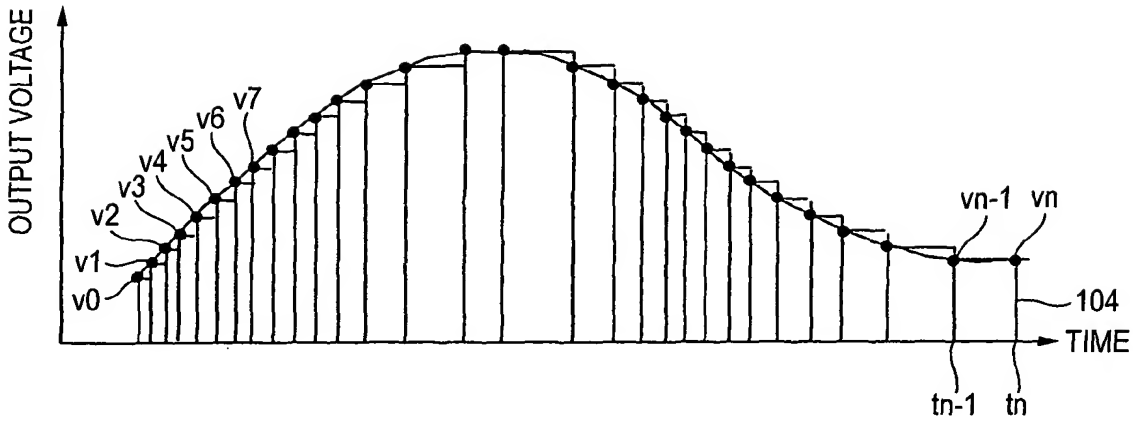


FIG. 2

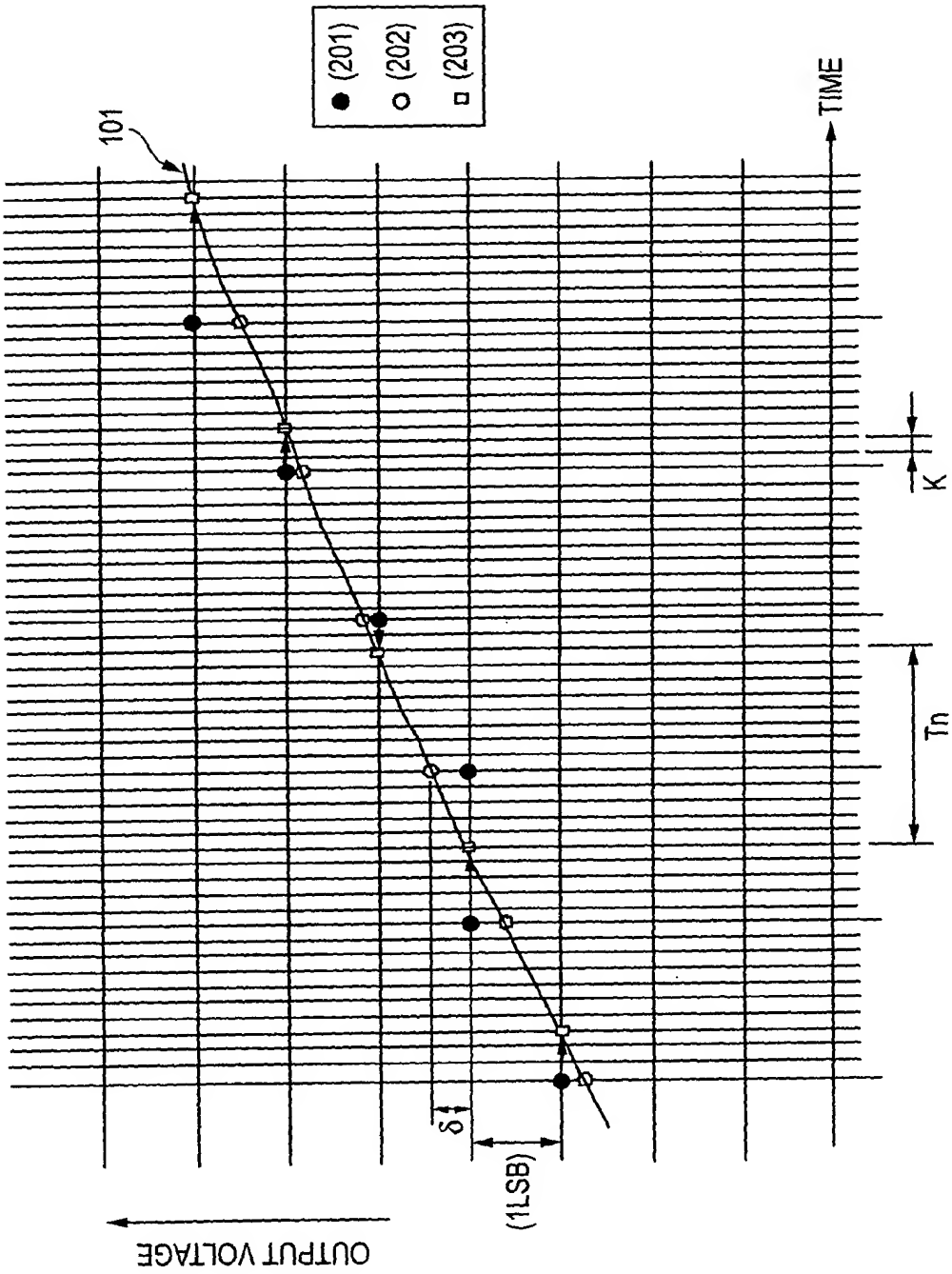


FIG. 3(a)

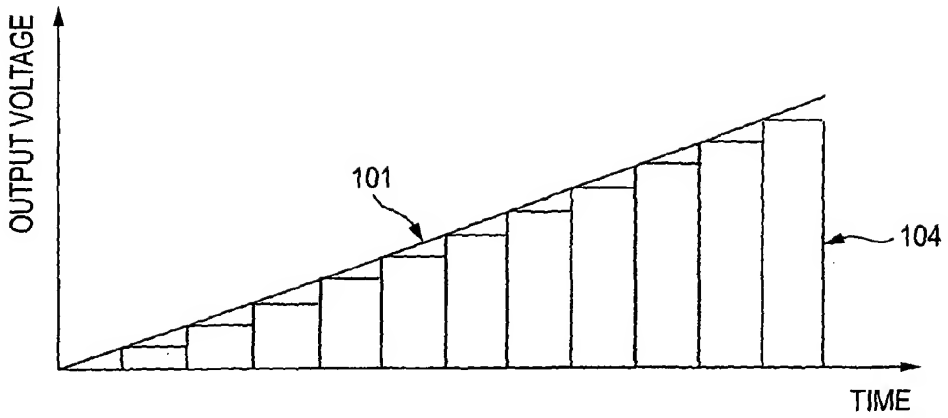


FIG. 3(b)

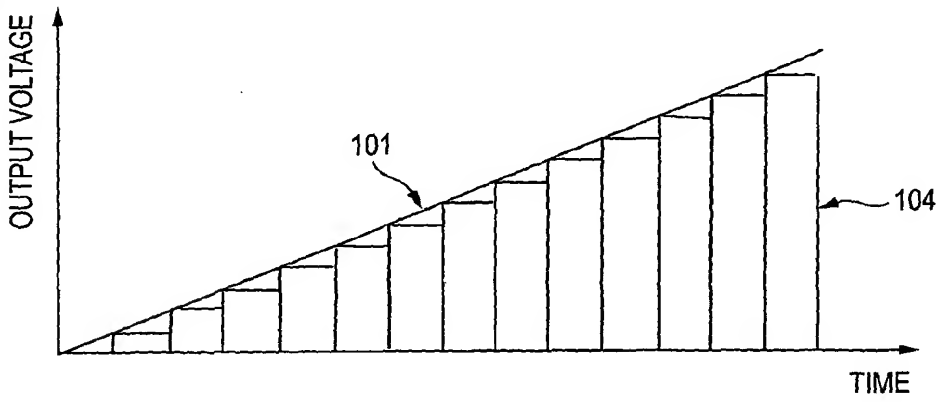


FIG. 3(c)

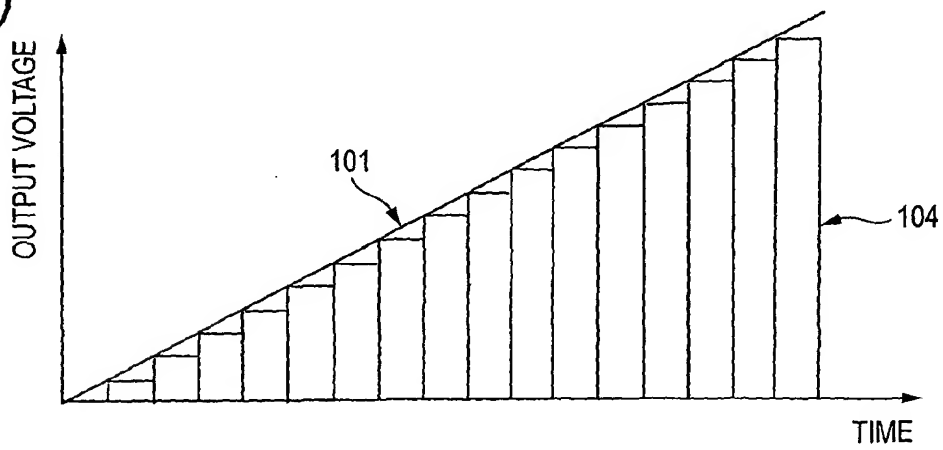


FIG. 4

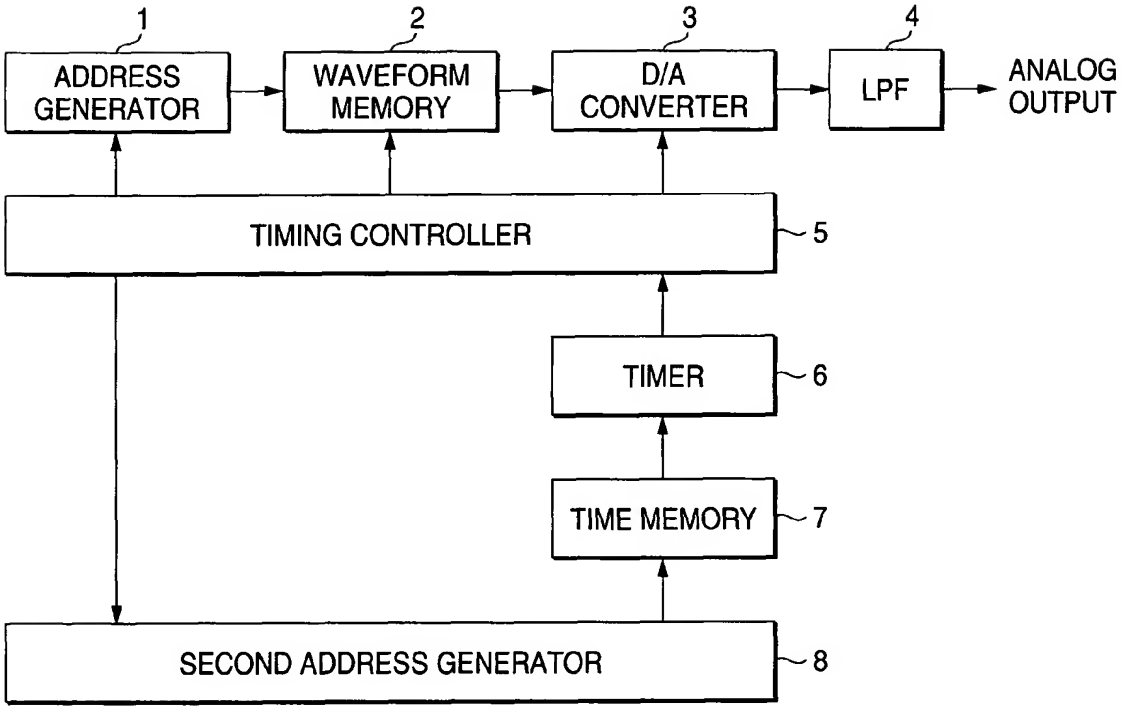

1
2
3
4
ADDRESS GENERATOR
WAVEFORM MEMORY
D/A CONVERTER
LPF
ANALOG OUTPUT
TIMING CONTROLLER
5
TIMER
6
TIME MEMORY
7
SECOND ADDRESS GENERATOR
8

FIG. 5

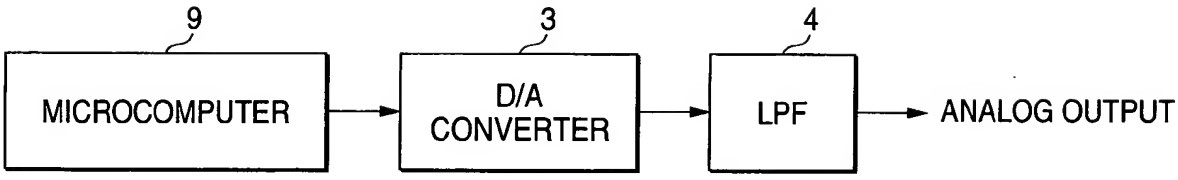


FIG. 6

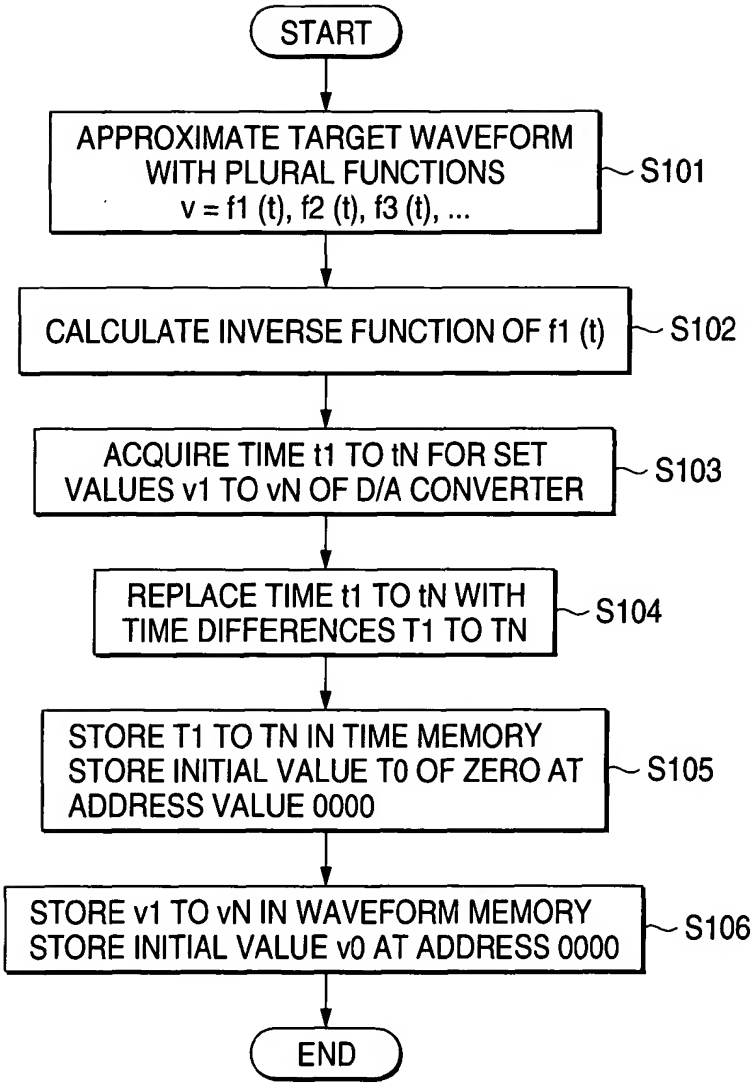

START
APPROXIMATE TARGET WAVEFORM WITH PLURAL FUNCTIONS v = f1 (t), f2 (t), f3 (t), ...
S101
CALCULATE INVERSE FUNCTION OF f1 (t)
S102
ACQUIRE TIME t1 TO tN FOR SET VALUES v1 TO vN OF D/A CONVERTER
S103
REPLACE TIME t1 TO tN WITH TIME DIFFERENCES T1 TO TN
S104
STORE T1 TO TN IN TIME MEMORY STORE INITIAL VALUE T0 OF ZERO AT ADDRESS VALUE 0000
S105
STORE v1 TO vN IN WAVEFORM MEMORY STORE INITIAL VALUE v0 AT ADDRESS 0000
S106
END

FIG. 7 (a)

TIME MEMORY	
ADDRESS	DATA
0000	0
0001	T1
0002	T2
0003	T3
0004	T4
⋮	⋮
N - 1	TN - 1
N	TN

7

FIG. 7 (b)

WAVEFORM MEMORY	
ADDRESS	DATA
0000	V0
0001	V1
0002	V2
0003	V3
0004	V4
⋮	⋮
N - 1	VN - 1
N	VN

2

FIG. 8

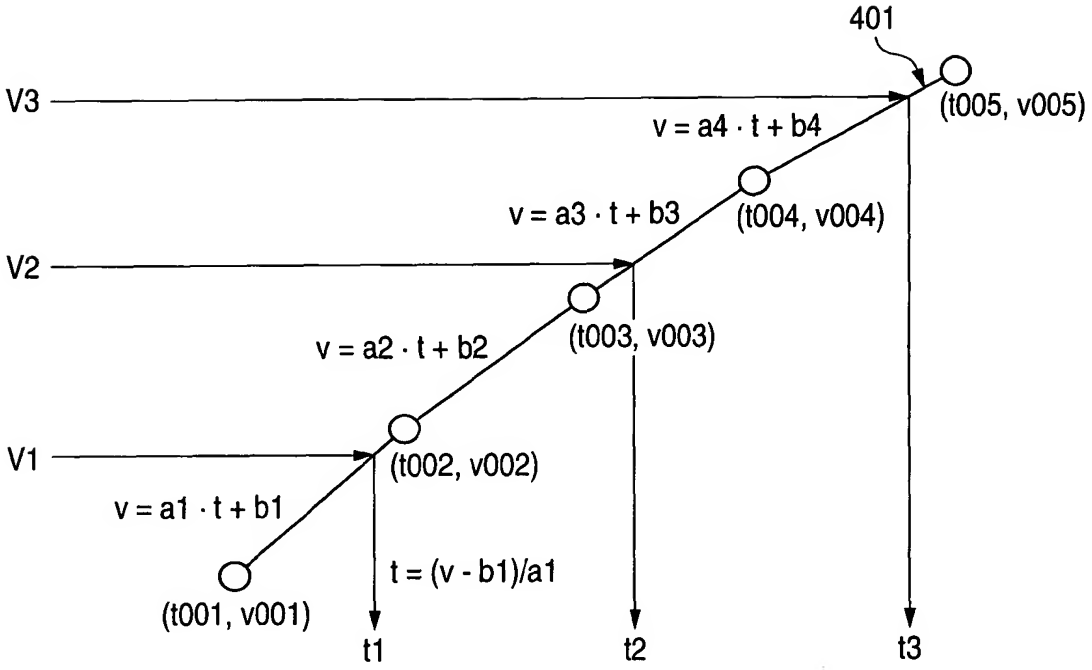

401
V3
V2
V1
(t005, v005)
v = a4 · t + b4
(t004, v004)
v = a3 · t + b3
(t003, v003)
v = a2 · t + b2
(t002, v002)
v = a1 · t + b1
(t001, v001)
t = (v - b1)/a1
t1
t2
t3

FIG. 9

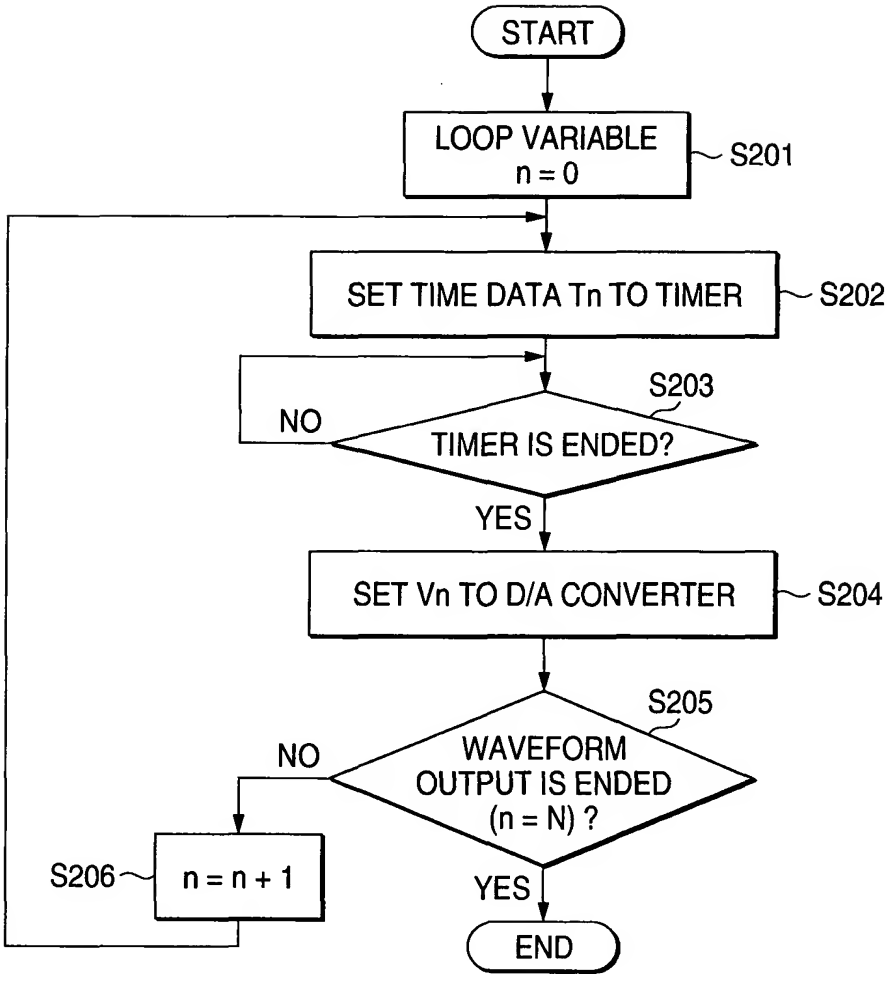

START
LOOP VARIABLE
n = 0
S201
SET TIME DATA Tn TO TIMER
S202
S203
NO
TIMER IS ENDED?
YES
SET Vn TO D/A CONVERTER
S204
S205
NO
WAVEFORM
OUTPUT IS ENDED
(n = N) ?
S206
n = n + 1
YES
END

FIG. 10 (a)

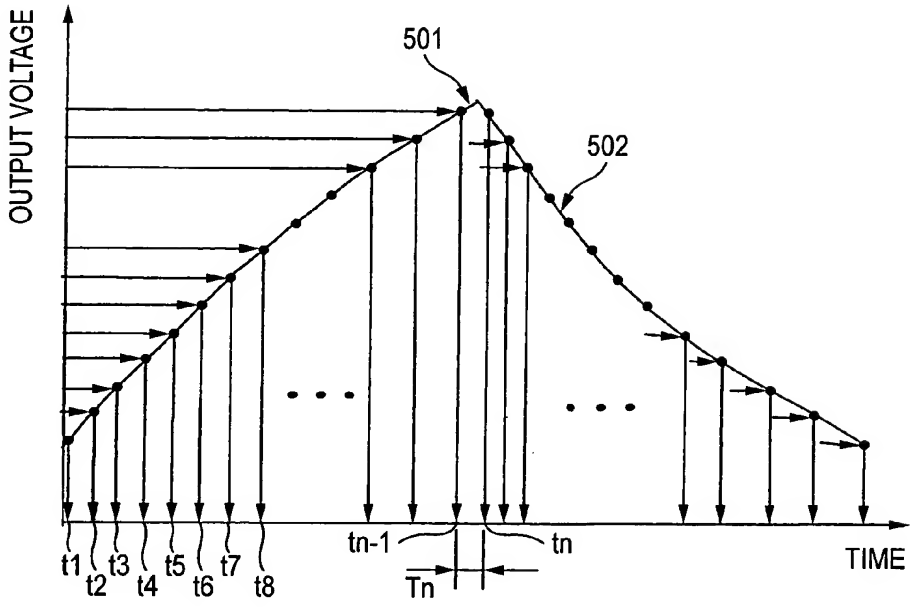


FIG. 10 (b)

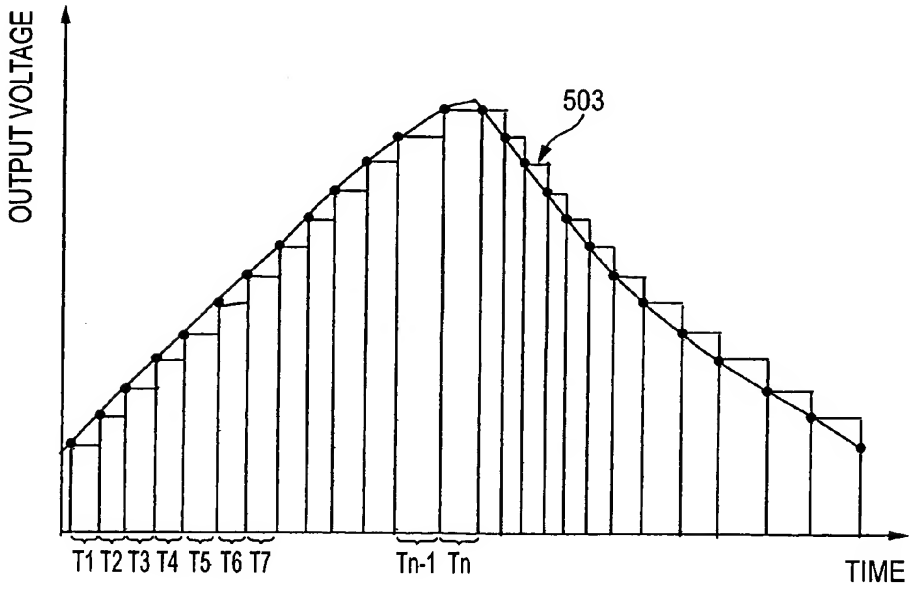


FIG. 11

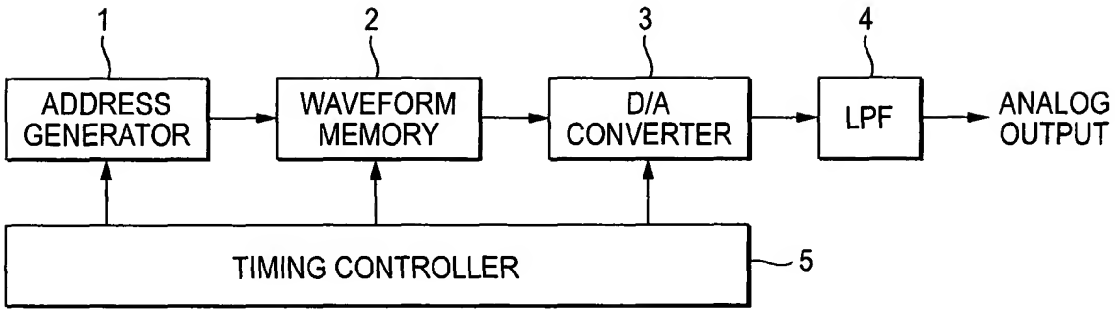

1
2
3
4
ADDRESS GENERATOR
WAVEFORM MEMORY
D/A CONVERTER
LPF
ANALOG OUTPUT
TIMING CONTROLLER
5

FIG. 12

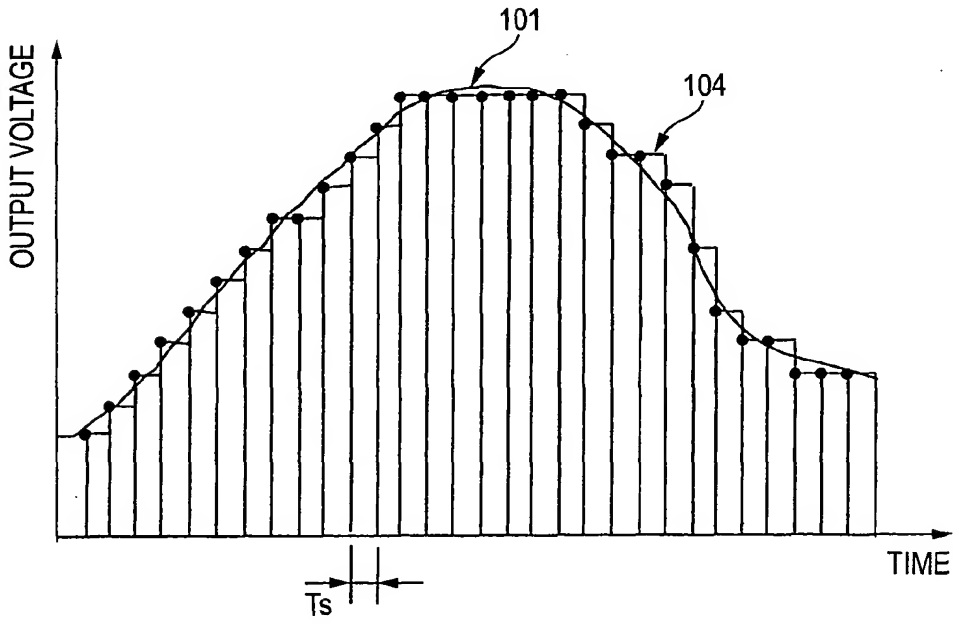

101
104
OUTPUT VOLTAGE
TIME
Ts

FIG. 13

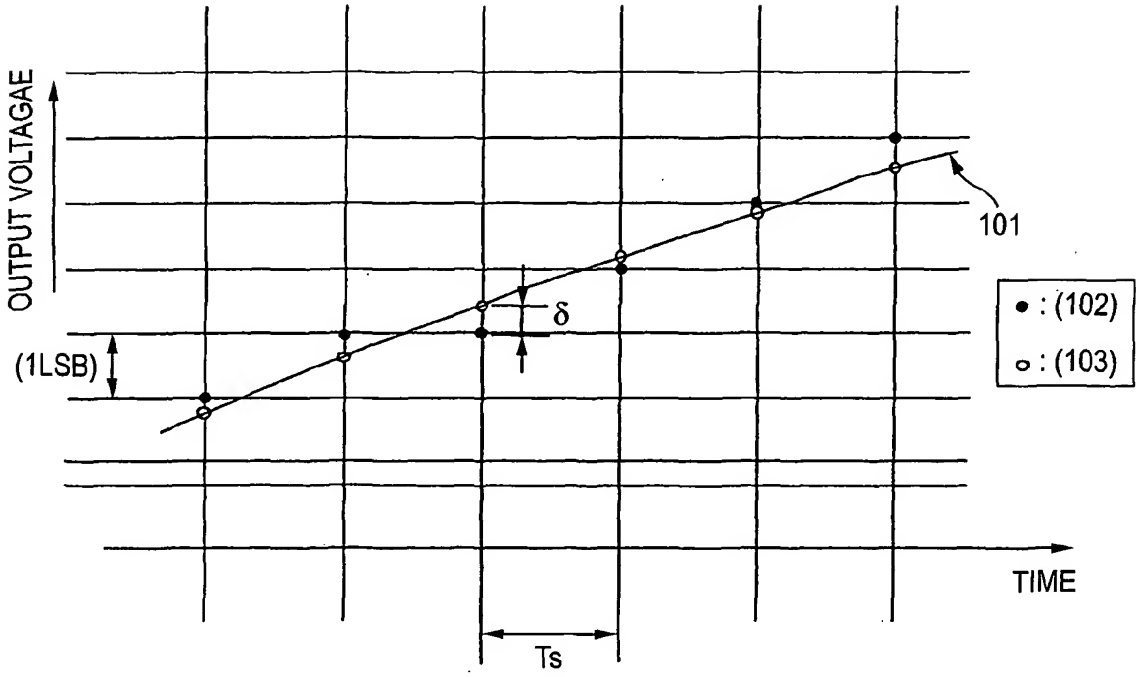


FIG. 14

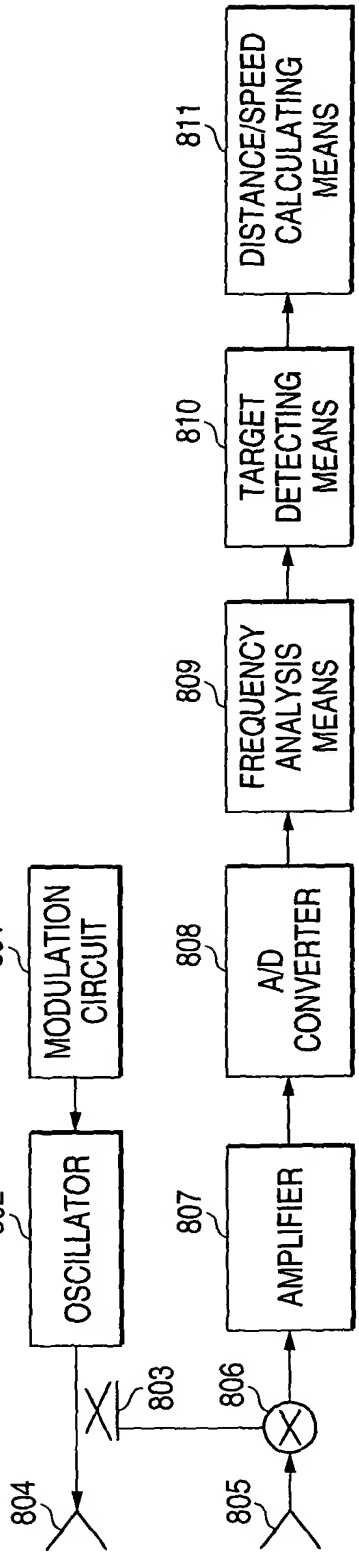

801
MODULATION CIRCUIT
802
OSCILLATOR
803
804
805
806
807
AMPLIFIER
808
A/D CONVERTER
809
FREQUENCY ANALYSIS MEANS
810
TARGET DETECTING MEANS
811
DISTANCE/SPEED CALCULATING MEANS

FIG. 15

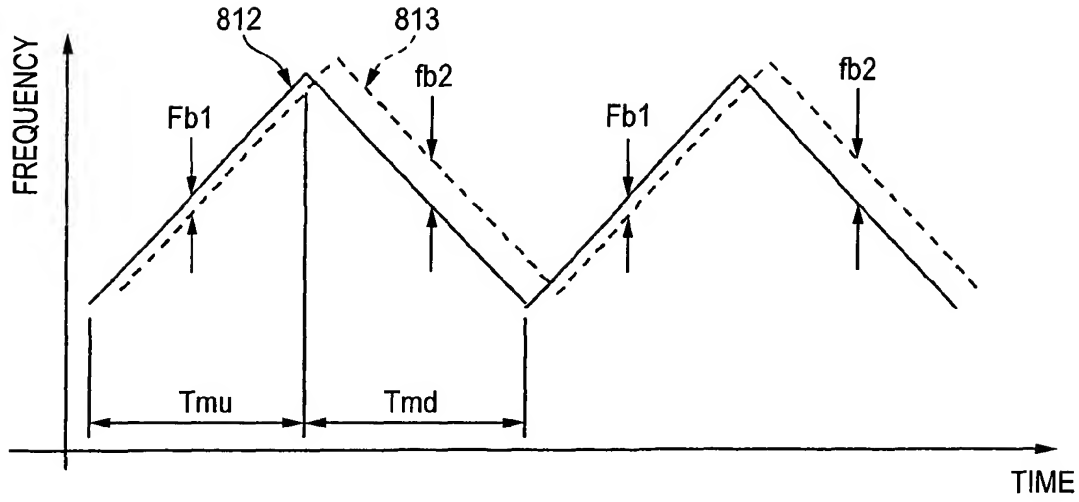


FIG. 16(a)

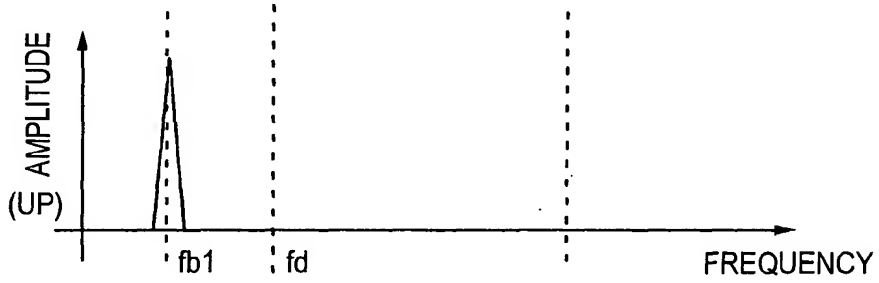


FIG. 16(b)

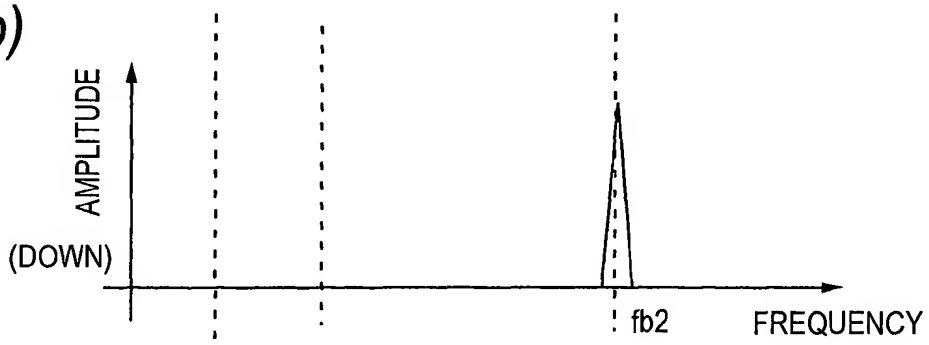


FIG. 17(a)

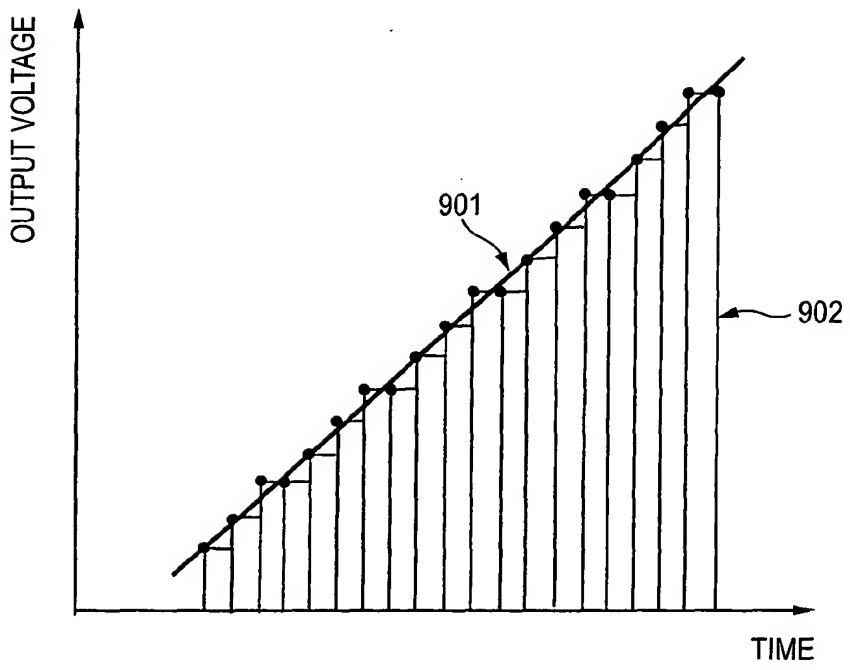


FIG. 17(b)

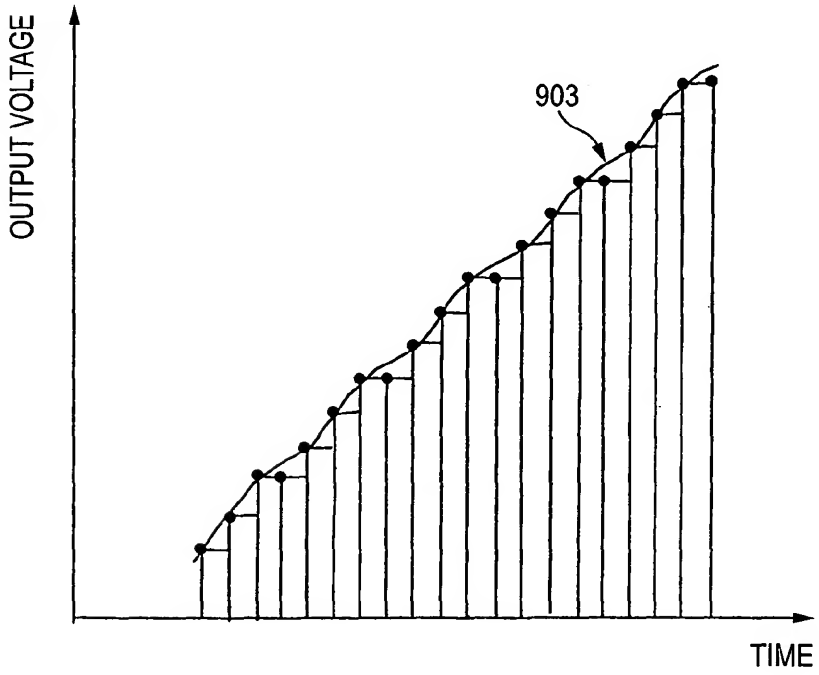


FIG. 18(a)

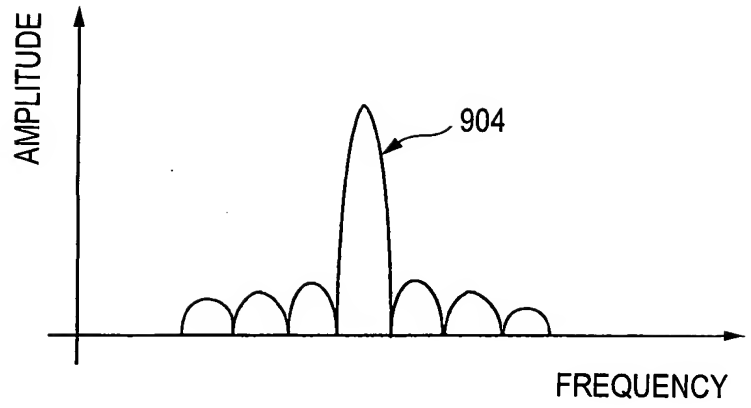


FIG. 18(b)

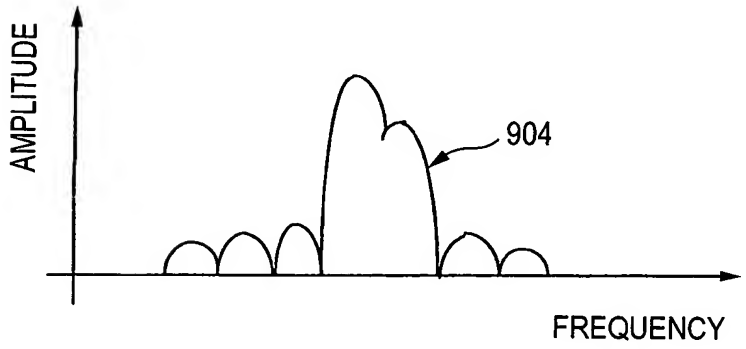
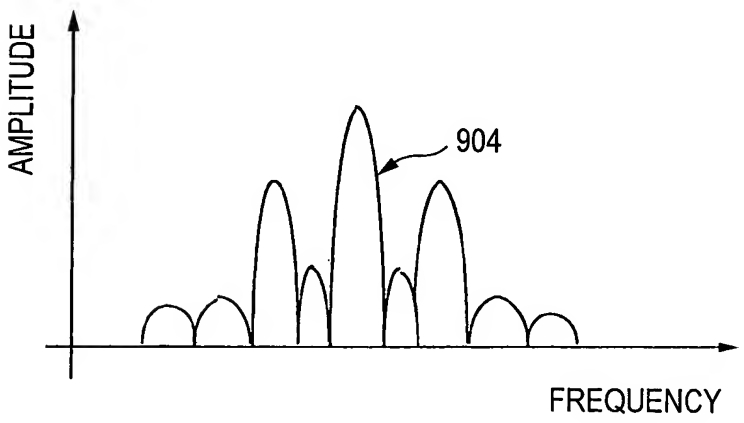


FIG. 18(c)



INTERNATIONAL SEARCH REPORT

International application No.
PCT/JP03/10702

A. CLASSIFICATION OF SUBJECT MATTER
Int.Cl[7] H03M1/66, H03B28/00, G01S7/282, G01S7/35, G01S13/34

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
Int.Cl[7] H03M1/00-H03M1/88, H03B28/00, G01S7/282, G01S7/35, G01S13/34

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Jitsuyo Shinan Koho	1926-1996	Toroku Jitsuyo Shinan Koho	1994-2003
Kokai Jitsuyo Shinan Koho	1971-2003	Jitsuyo Shinan Toroku Koho	1996-2003

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X Y A	Microfilm of the specification and drawings annexed to the request of Japanese Utility Model Application No. 42717/1989(Laid-open No. 134723/1990) (Yokogawa Electric Corp.), 08 November, 1990 (08.11.90), Full text; all drawings (Family: none)	1,2 4-6 3
X Y A	JP 61-144930 A (Hitachi, Ltd.), 02 July, 1986 (02.07.86), Full text; all drawings (Family: none)	1,2 4-6 3

☒ Further documents are listed in the continuation of Box C. ☐ See patent family annex.

* Special categories of cited documents:
"A" document defining the general state of the art which is not considered to be of particular relevance
"E" earlier document but published on or after the international filing date
"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)
"O" document referring to an oral disclosure, use, exhibition or other means
"P" document published prior to the international filing date but later than the priority date claimed
"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
26 November, 2003 (26.11.03)	09 December, 2003 (09.12.03)
Name and mailing address of the ISA/ Japanese Patent Office Facsimile No.	Authorized officer Telephone No.

Form PCT/ISA/210 (second sheet) (July 1998)

INTERNATIONAL SEARCH REPORT

International application No.
PCT/JP03/10702

C (Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	JP 11-168325 A (Sony Corp.), 22 June, 1999 (22.06.99), Column 1, line 50 to column 2, line 24; column 6, lines 31 to 48; column 12, line 34 to column 14, line 39; column 15, line 26 to column 16, line 9; Figs. 5, 6 (Family: none)	4-6

Form PCT/ISA/210 (continuation of second sheet) (July 1998)

PUB-NO: EP001533906A1

DOCUMENT-IDENTIFIER: EP 1533906 A1

TITLE: WAVEFORM GENERATION METHOD, WAVEFORM GENERATION PROGRAM, WAVEFORM GENERATION CIRCUIT, AND RADAR DEVICE

PUBN-DATE: May 25, 2005

INVENTOR-INFORMATION:

NAME	COUNTRY
INATSUNE, SHIGEHO	JP

ASSIGNEE-INFORMATION:

NAME	COUNTRY
MITSUBISHI ELECTRIC CORP	JP

APPL-NO: EP03792829

APPL-DATE: August 25, 2003

PRIORITY-DATA: JP2002244918A (August 26, 2002)

INT-CL (IPC): H03M001/66 , H03B028/00 , G01S007/282 , G01S007/35 , G01S013/34

ABSTRACT:

CHG DATE=20050531 STATUS=O>A conventional waveform generation circuit was required to increase a number of bits or a sampling rate for a D/A converter to enhance a precision of

waveform shaping, and had a problem that a cost was increased. Therefore, as a method for enhancing the precision of waveform shaping, a quantization error of an output waveform is made smaller by controlling an output time interval of an output value from a D/A converter so as to make a difference in an output voltage between target waveform and output waveform smaller. As a result, even if the D/A converter has a small number of bits, the waveform can be generated at high precision. Also, this waveform generation method may be applied to modulation control of a radar apparatus, as a result, constituting a small and inexpensive modulation circuit for an oscillator.